REMARKS

Reconsideration of the above-identified patent application is requested in view of the remarks that follow.

In the July 3, 2001, Office Action in this application, the Examiner rejected claims 39-48 under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner cited specific §112 deficiencies with respect to each of claims 39, 42, and 48.

As indicated above, claims 39-48 have been cancelled in favor of corresponding new claims 49-58. Thus, new claim 49 corresponds to cancelled claim 39; new claim 52 corresponds to cancelled claim 42; and new claim 58 corresponds to cancelled claim 48.

Each of new claims 49, 52 and 58 has been drafted with the Examiner's Section 112 concerns regarding respective cancelled claims 39, 42 and 48 in mind. Specifically, with respect to cancelled claim 39, the Examiner has stated that reference to "each solder ball" should apparently be "conductive solder ball"; new claim 49 has been drafted to replace the term "each solder ball" with "conductive solder ball." With respect to cancelled claim 42, the Examiner stated that there is no support in Applicant's specification for the limitation of "each ... die having a scribed portion of said glass sheet affixed"; as indicated above, new claim 52 has been drafted to recite that the semiconductor integrated circuit wafer scale structure is disposed to be "cut" along scribed lines to provide a plurality of individual integrated circuit die structures. With respect to cancelled claim 48, the Examiner questions whether reference to "conductive bond pad" on line 4 is the same pad as the die bond pad referenced at line 11 of the claim; as indicated above, claim 58 has been drafted to draw a clear distinction between conductive die bond pads and conductive solder ball bond pad structures.

Thus, it is believed that all new claims currently pending in this application are in compliance with all requirements of 35 U.S.C. §112.

The Examiner also rejected claims 39-48 under 35 U.S.C. §103(a) as being unpatentable over the Kata et al. reference in view of the Lin reference, the Tsukamoto reference and the Igarashi et al. reference. For the reasons set forth below, the §103 rejection is traversed as it may

As stated above, new claims 49-58 correspond to cancelled claims 39-48. However, each of Applicant's new independent claims 49, 57 and 58 has been drafted to clarify three key features which, it is believed, patentably distinguish the claimed invention over the prior art reference combination cited by the Examiner.

First, each of independent claims 49, 57 and 58 has been drafted to recite as an element a unitary, substantially planar glass sheet. That is, Applicant wishes to clarify that the glass sheet recited in each of these claims is a single, unitary structure having independent integrity and a substantially planar configuration prior to its being affixed to the underlying semiconductor wafer substrate. In the reference combination cited by the Examiner, the Examiner seeks to equate the plate 22 taught by the Lin patent to the unitary, substantially planar single glass sheet recited in Applicant's new independent claims. However, with particular reference to Applicant's Figs. 1A-1D, Applicant submits that there is very little similarity between the unitary, substantially planar glass sheet 100, which, as is also recited in each of independent claims 49, 57 and 58, is substantially the same size as the semiconductor wafer substrate 106, and the plate 22 disclosed by Lin. Furthermore, there is no motivation provided in any of the references to substitute Lin's plate 22 for the spun-on cover coating film 64 of the Kata et al. reference as would be required to achieve the structural combination proposed by the Examiner.

Second, each of new independent claims 49, 57 and 58 recites that the glass sheet includes a plurality of prefabricated holes that are formed through the glass sheet from an upper surface of the glass sheet to a lower surface of the glass sheet. The holes in the glass sheet are defined as being "prefabricated" to emphasize that the holes are formed in the glass sheet prior to the glass sheet being affixed to the semiconductor wafer substrate. This feature of Applicant's invention is clearly shown in Applicant's Fig. 1B.

Third, and significantly, each of Applicant's new independent claims 49, 57 and 58 recites an adhesive material that is disposed between the semiconductor wafer substrate and the glass sheet to affix the glass sheet to the semiconductor wafer substrate. The Examiner refers to the Igarashi et al. reference as showing the use of a polyimide to bond a die to an intermediate sheet. Applicant assumes that the Examiner is referring to the use of polyimide resin layer 3 to adhere a semiconductor chip 1 to an auxiliary wiring plate 2. However, as discussed further in

Applicant submits that not only is the Igarashi et al. structure directed to an integrated circuit die level structure, rather than to a wafer scale structure as recited in each of Applicants' new independent claims, but also the components referred to by the Examiner are completely dissimilar to those referred to and defined in Applicant's new independent claims 49, 57 and 58.

Applicant submits that the Examiner is attempting to pick and choose structural features from a plurality of references in an attempt to reconstruct the claimed invention, but only with the impermissible hindsight benefit provided by applications specification, claims and drawings. Furthermore, Applicant respectfully submits that the Examiner is engaging in a tortuous effort to cram the die level features of the Lin, Tsukamoto and Igarashi et al. references into the wafer level environment disclosed by Kata et al. that is not suggested by any of the references, and which would only be attempted, if at all, with the hindsight benefit provided by Applicant's specification, claims and drawings.

For the reasons set forth above, Applicant submits that all claims now present in this application are incompliance with all requirements of 35 U.S.C. §112 and patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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